

Appl. No. 09/912,810  
Amdt. dated June 22, 2005  
Reply to Office action of February 22, 2005

## PATENT

## IN THE CLAIMS

This listing of claims will replace all prior versions, and listings, of claims in the application:

## Listing of Claims:

1. (Currently Amended) An apparatus for dithering pixel data, comprising:  
a dither value generator for outputting a dither reference value in response to an N-bits pixel data and a pixel address (x,y) thereof, wherein the dither value generator includes:  
a dither matrix; and  
an array index generator for generating an array index (i, j) in response to the N-bits pixel data and the pixel address (x,y) as follows: i = (x+C) modulo n; j = (y+C) modulo n,  
wherein C denotes the red, green or blue color value of the pixel to be dithered and n represents the dimension of the dither matrix; and  
a dithering unit for generating an M-bits pixel data in response to the dither reference value and the N-bits pixel data;  
wherein the value N is greater than the value M.
2. (Currently Amended) The apparatus of claim 1, wherein said dither value generator further comprises:  
a dither matrix;  
an array index generator for generating an array index (i, j) in response to the N-bits pixel data and the pixel address (x, y) as follows: i = (x+C) modulo n; j = (y+C) modulo n, wherein C denotes the red, green or blue color value of the pixel to be dithered; and  
a selecting unit for selecting the dither reference value from said dither matrix in response to the array index (i, j) generated by said array index generator.
3. (Original) The apparatus of claim 1, wherein said dithering unit comprises:  
a truncating unit for generating the M-bits pixel data by truncating the (N-M) least significant bits of the N-bits pixel data;  
a comparing unit for outputting a comparison signal by comparing the (N-M) least significant bits of the N-bits pixel data with the dither reference value;

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an adder for adding the M-bits pixel data to the comparison signal, and outputting a "sum" signal and an "overflow" signal; and

a clamping unit for performing a clamping process on the "sum" signal in response to the "overflow" signal, and outputting the M-bits pixel data.

4. (Original) An apparatus for inversely dithering pixel data comprising:

a dither value generator for generating a (N-M) bits dither reference value in response to a dithered M-bits pixel data and a pixel address (x, y); and

an inversely dithering unit for converting the dithered M-bits pixel data to original N-bits pixel data in response to the dither reference value and the dithered M-bits pixel data, wherein the value N is greater than the value M.

5. (Currently Amended) The apparatus of claim 4, wherein said dither value generator comprises:

a dither matrix;

an array index generator for generating an array index (i, j) in response to the dithered M-bits pixel data and the pixel address (x, y) as follows: I = (x+C) modulo n; j = (y+C) modulo n, wherein C denotes the red, green or blue color value of the pixel to be inversely dithered and n represents the dimension of the dither matrix; and

a selecting unit for selecting a dither reference value from said dither matrix in response to the array index (i, j) generated by said array index generator.

6. (Original) The apparatus of claim 4, wherein said inversely dithering unit comprises:

an appending unit for appending the (N-M) bits dither reference value to the dithered M-bits pixel data and generating an N-bits pixel data;

a subtracting unit for subtracting a constant value from the output N-bits pixel data of said appending unit and outputting a "difference" signal and an "overflow" signal; and

a clamping unit for performing a clamping process on the "difference" signal in response to the "overflow" signal, and outputting the N-bits pixel data.

7. (Original) The apparatus of claim 6, wherein the value of a is  $2^{(N-M)/2}$ .

8. (New) An apparatus for dithering pixel data, comprising:

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a dither value generator for outputting a dither reference value in response to an N-bits pixel data and a pixel address (x, y) thereof; and

a dithering unit for generating an M-bits pixel data in response to the dither reference value and the N-bits pixel data, wherein said dithering unit comprises:

a truncating unit for generating the M-bits pixel data by truncating the (N-M) least significant bits of the N-bits pixel data;

a comparing unit for outputting a comparison signal by comparing the (N-M) least significant bits of the N-bits pixel data with the dither reference value;

an adder for adding the M-bits pixel data to the comparison signal, and outputting a "sum" signal and an "overflow" signal; and

a clamping unit for performing a clamping process on the "sum" signal in response to the "overflow" signal, and outputting the M-bits pixel data;

wherein the value N is greater than the value M.